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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/048,933	03/26/1998	DEAN A. KLEIN	MEI-97-01386	4879

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EXAMINER
LO, LINUS H

ART UNIT	PAPER NUMBER
2614	

DATE MAILED: 05/08/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/048,933	Applicant(s) KLEIN, DEAN A.	
	Examiner Linus H Lo	Art Unit 2614	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *2/19/2002,Req. CPA and Pre. Amend.* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 12-19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-10 and 12-19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *8/8/2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Continued Prosecution Application

1. The request filed on 2/19/2002 for a Continued Prosecution Application (CPA) under 37 CFR 1.53(d) based on parent Application No. 09/048,933 is acceptable and a CPA has been established. An action on the CPA follows.

2. It is noted the mark up version of the amendment, does not fully correspond to the clean copy of the amended claims , i.e. the limitation of " wherein the core logic chip is a semiconductor chip ... for the computer system" is not recited in the mark-up copy. Thus for the response purpose the limitation of " wherein the core logic chip is a semiconductor chip ... for the computer system" is considered to be included in the amendment.

Claim Rejections - 35 USC § 103

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

4. Claims 1-3, 5-7, 10 and 12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dea '208 (of record) in view of Potu '651 (New)

Considering claim 1(Twice Amended), Dea discloses a remote video processing system including compression/decompression accelerator. Dea discloses the following claimed subject matter, note:

a) the claimed method for compressing video data in a computer system is met by the description at column 4, lines 36-41 and lines 17-19, and FIG. 1, where of the described compression/decompression accelerator 120 performs the compression method;

b) the claimed step of receiving a stream of data from a current video frame in the computer system is met by description at column 6, lines 42-44 and FIG. 2;

c) the claimed step of computing a difference frame from the current video frame and a previous video frame as the current video frame streams into the computer system is met by the description of the subtraction function of frame difference block 220 (column 6, lines 36-44, and column 5, lines 42-47, and FIG. 2);

d) the claimed step of storing difference frame in a memory in the computer system is met by the description of buffer 248 at column 9, line 60 - column 10, line 3, and FIG. 2;

e) the teaching of "wherein computing the difference fame includes computing the difference frame in **a core logic unit** within the computer system" as described by the compress/decompression accelerator 120 that includes the function frame difference block 220 (column 6, lines 36-44, and column 5, lines 42-47, and FIG.1, 2); and

f) the teaching of "the **core logic unit** that couples the processor to a main memory and a system bus for the computer system" as depicted on Fig. 1 and column 4, lines 37-60, where Fig. 1 depicts the compress/decompression accelerator 120 (core logic unit) is coupled to processor 112 and DRAM 114 through the data and system but 116, 118.

However, Dea does not explicitly teach the claimed computing the difference frame in a ***core logic chip*** , wherein ***the core logic chip is a semiconductor chip*** as recited. Nonetheless, Dea teaches the computing the difference frame in a compression/depression accelerator 120 (core logic unit) as discussed above in points (e) and (f).

Potu teaches an apparatus for transferring a video image , to be resized , from host processor to an accelerator chip of a display adapter. Potu discloses that video accelerator (core logic unit) is in the form of video accelerator chip as described in column 1, lines 54-63. Since video accelerator (core logic unit) is in the form of a semiconductor chip which is an equivalent structure known in the art which is further demonstrated by the teaching of Potu. Therefore it would have been obvious to one having ordinary skilled in the art at the time the invention was made to substitute the **accelerator in the chip form** as taught by Potu for the accelerator 120 (core logic unit) as in the system of Dea.

Considering claim 2, the claimed storing the current video frame in the memory in the computer system is met by the current frame memory 204 (column 6, lines 42-44, and FIG. 2).

Considering claim 3, the claimed wherein the current video frame is written over a previous video frame in the memory is met by the current frame memory 204 (column 6, lines 42-44, and FIG. 2.), whereas the current frame memory 204 receives video frame sequentially that the area stores the relatively previous video frame is subsequently replace by the newly received current video frame.

Considering claim 5, the claimed step of computing a difference between a block of data from the current video frame and a block of data from the previous video frame is met description at column 10 , lines 53-56 and column 5, lines 42-47, and FIG. 3A, where the excerpt from column 10 described the utilizing of the block of data from the current and previous video frame.

Considering claim 6, the claimed wherein storing the difference frame in memory includes storing the differences frame in the memory in the memory using block transfer is met by the is met the description at column 10 , lines 53 - column 11, lines7 and column 5, lines 42-47, and FIG. 3A, where the excerpt from column 10 and 11 described the utilizing of the block of data from the current and previous video frame and subsequently recognized that data stored in buffer is in the from of block.

Considering claim 7, the claimed using the difference frame to produce compressed video data is met by the description of FIG. 3A and column 10, line 53 - column 11, line 7, whereof FIG. 3A depicted the frame difference block 220 provides a difference frame and subsequently after the variable length encoding block , the compressed video bitstream 338 is output.

Considering claim 10, the system of Dea and Potu discloses the claimed invention except for the claimed storing instruction and data for the computer system in the memory.

Nevertheless, Dea teaches *a step of storing* data for the computer system in the memory as the description of DRAM at column 4, lines 52-63, and furthermore Dea teaches that the video processing system 100 (computer system) utilizes executable program instructions (column 4, lines 36-51). Since examiner takes Official Notice of the commonly known in the art that processing system (computer system) stores instruction for the computer system in the memory in order for the system to retrieve and executed the programmed instruction would be within the level of ordinary skill in the art . Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize the claimed step of storing instruction and data for the computer system in the memory in the system of Dea and Potu.

Considering claim 12, the claimed wherein computing the difference frame includes computing the difference frame in circuitry outside of a central processing unit in the

computer system is met by the processor 112 and the compression/decompression accelerator 120 (FIG. 2).

5. Claims 4, 9, 13-17, and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Dea '208 (of record) and Potu '651(New), and further in view of Abramatic et al. '383 (of record).

Considering claim 4, the system of Dea and Potu discloses the claimed invention except for the claimed step of computing the difference frame includes computing an exclusive-OR between the current video frame and the previous video frame.

Nonetheless, Dea teaches that a step of computing *the difference frame* between the current video frame and the previous video frame as discuss above in claim 1. Furthermore, Abramatic et al. teach that a form of compression consists in detecting variations (difference) between on image and the next as described at column 2, lines 53-56. Abramatic et al. discloses the claimed step of computing an exclusive-OR between the current video frame and the previous video frame as met by the description at column 6, lines 52-58, whereof the described previous image at the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video frame.

Since Abramatic et al. teach that XOR function for the difference calculation 56 which has the advantage of providing a less complicated means for the difference calculation techniques as elucidate at column 7, lines 32-35.

Therefore it would have been obvious to one have ordinary skilled in the art at the time the invention was made to recognize the advantage and the claimed the claimed step of computing the difference frame includes computing an exclusive-OR between the current video frame and the previous video frame as taught by Abramatic et al. in the system of Dea and Potu .

Considering claim 9, the system of Dea and Potu discloses the claimed invention except for the claimed using the video data in compressed form in a video teleconferencing system.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize the claimed using the video data in compressed form in a video teleconferencing system in the system of Dea and Potu , since examiner takes Official Notices of the commonly well known usage of the compressed video data form in a teleconference system , whereof the compressed video data form is recognized to provide the benefit of bandwidth conservation on a communication system.

Considering claim 13(Twice Amended), Dea discloses a remote video processing system including compression/decompression accelerator. Dea discloses the following claimed subject matter, note:

a) the claimed method for compressing video data in a computer system is met by the description at column 4, lines 36-41 and lines 17-19, and FIG. 1, where of the described compression/decompression accelerator 120 performs the compression method;

b) the claimed step of receiving a stream of data from a current video frame in the computer system is met by description at column 6, lines 42-44 and FIG. 2;

c) the claimed step of computing a difference frame from the current video frame and a previous video frame as the current video frame streams into the computer system is met by the description of the subtraction function of frame difference block 220 (column 6, lines 36-44, and column 5, lines 42-47, and FIG. 2);

d) the claimed step of storing difference frame in a memory in the computer system is met by the description of buffer 248 at column 9, line 60 - column 10, line 3, and FIG. 2;

e) the claimed storing the current video frame in the memory in the computer system is met by the current frame memory 204 (column 6, lines 42-44, and FIG. 2);

f) the claimed using the difference frame to produce compressed video data is met by the description of FIG. 3A and column 10, line 53 - column 11, line 7, whereof FIG. 3A depicted the frame difference block 220 provides a difference frame and subsequently after the variable length encoding block , the compressed video bitstream 338 is output; and

g) the teaching of "wherein computing the difference fame includes computing the difference frame in **a core logic unit** within the computer system" as described by the compress/decompression accelerator 120 of Dea that includes the function frame difference block 220 (column 6, lines 36-44, and column 5, lines 42-47, and FIG.1, 2).

h) the teaching of "the **core logic unit** that couples the processor to a main memory and a system bus for the computer system" as depicted on Fig. 1 and column 4, lines 37-60, where Fig. 1 depicts the compress/decompression accelerator 120 (core logic unit) is coupled to processor 112 and DRAM 114 through the data and system but 116, 118.

However, Dea does not explicitly disclose, note :

i) the claimed computing the difference frame in a ***core logic chip*** , wherein ***the core logic chip is a semiconductor chip*** as recited, and

ii) the claimed step of computing the difference frame includes computing an exclusive-OR between the current video frame and the previous video frame

Regarding **(i)**, Dea teaches the computing the difference frame in a compression/depression accelerator 120 (core logic unit) as discussed above in points (g) and (h).

Potu teaches an apparatus for transferring a video image , to be resized , from host processor to an accelerator chip of a display adapter. Potu discloses that video accelerator (core logic unit) is in the form of **video accelerator chip** as described in column 1, lines 54-63. Since video accelerator(core logic unit) is in the form of **a semiconductor chip** which is an equivalent structure known in the art which is further demonstrated by the teaching of Potu. Therefore it would have been obvious to one having ordinary skilled in the art at the time the

invention was made to substitute the **accelerator in the chip form** as taught by Potu for the accelerator 120 (core logic unit) in the system of Dea.

Regarding **(ii)**, Dea teaches a step of computing *the difference frame* between the current video frame and the previous video frame as discuss above in claim 1. Furthermore, Abramatic et al. teach that a form of compression consists in detecting variations (difference) between on image and the next as described at column 2, lines 53-56. Abramatic et al. discloses the claimed step of computing an exclusive-OR between the current video frame and the previous video frame as met by the description at column 6, lines 52-58, whereof the described previous image at the input 55 and the arrival of new points at the input 57 which are respectively considered as the previous and current video frame.

Since Abramatic et al. teach that XOR function for the difference calculation 56 which has the advantage of providing a less complicated means for the difference calculation techniques as elucidate at column 7, lines 32-35.

Therefore it would have been obvious to one have ordinary skilled in the art at the time the invention was made to recognize the advantage and the claimed step of computing the difference frame includes computing an exclusive-OR between the current video frame and the previous video frame as taught by Abramatic et al. in the system of Dea and Potu.

Considering claim 14, the claimed wherein the current video frame is written over a previous video frame in the memory is met by the current frame memory 204 of Dea (column 6, lines 42-44, and FIG. 2.), whereas the current frame memory 204 receives video frame

sequentially that the area stores the relatively previous video frame is subsequently replace by the newly received current video frame.

Considering claim 15, the claimed step of computing a difference between a block of data from the current video frame and a block of data from the previous video frame is met description of Dea at column 10 , lines 53-56 and column 5, lines 42-47, and FIG. 3A, where the excerpt from column 10 described the utilizing of the block of data from the current and previous video frame.

Considering claim 16, the claimed wherein storing the difference frame in memory includes storing the differences frame in the memory in the memory using block transfer is met by the is met the description of Dea at column 10 , lines 53 - column 11, lines7 and column 5, lines 42-47, and FIG. 3A, where the excerpt from column 10 and 11 described the utilizing of the block of data from the current and previous video frame and subsequently recognized that data stored in buffer is in the from of block.

Considering claim 17, the system of Dea and Potu discloses the claimed invention except for the claimed using the video data in compressed form in a video teleconferencing system.

It would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize the claimed using the video data in compressed form in a video teleconferencing system in the system of Dea and Potu , since examiner takes Official Notices

of the commonly well known usage of the compressed video data form in a teleconference system , whereof the compressed video data form is recognized to provide the benefit of bandwidth conservation on a communication system.

Considering claim 19, the system of Dea, Potu and Abramatic et al. discloses the claimed invention except for the claimed storing instruction and data for the computer system in the memory.

Nevertheless, Dea teaches *a step of storing* data for the computer system in the memory as the description of DRAM at column 4, lines 52-63, and furthermore Dea teaches that the video processing system 100 (computer system) utilizes executable program instructions (column 4, lines 36-51). Since examiner takes Official Notice of the commonly known in the art that processing system (computer system) stores instruction for the computer system in the memory in order for the system to retrieve and executed the programmed instruction would be within the level of ordinary skill in the art . Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize the claimed step of storing instruction and data for the computer system in the memory in the system of Dea, Potu and Abramatic et al..

6. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dea '208 and Potu '651 as applied to claim 1 above, and further in view of Hardiman ' 223 (of record).

Considering claim 8, the system of Dea and Potu discloses the claimed invention except for the claimed step of performing a color space conversion on the video data.

Hardiman discloses an invention relates to compression coding of a video program. Hardiman disclose the claimed performing a color space conversion on the video data is met by the subsampler and color space converter 80 (column 3, lines 47-57, column 6, lines 55-64, and FIG. 2). Since it was well known in the art that the color space conversion on video would recognize the benefit of properly converting the video information from a computer processed information into a displayable signal for image displaying (column 3, lines 47-57).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize the advantage of performing a color space conversion on the video data and further realize the claimed step of performing a color space conversion on the video data as taught by Hardiman in the system of Dea and Potu .

7. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Dea ' 208 , Potu '651 and Abramatic et al. '383 as applied to claim13 above, and further in view of Hardiman '223.

Considering claim 18, the system of Dea , Potu and Abramatic et al. discloses the claimed invention except for the claimed step of performing a color space conversion on the video data.

Hardiman discloses an invention relates to compression coding of a video program. Hardiman disclose the claimed performing a color space conversion on the video data is met by the subsampler and color space converter 80 (column 3, lines 47-57, column 6, lines 55-64, and FIG. 2). Since it was well known in the art that the color space conversion on video would recognize the benefit of properly converting the video information from a computer processed information into a displayable signal for image displaying (column 3, lines 47-57).

Therefore it would have been obvious to one having ordinary skill in the art at the time the invention was made to recognize the advantage of performing a color space conversion on the video data and further realize the claimed step of performing a color space conversion on the video data as taught by Hardiman in the system of Dea, Potu and Abramatic et al..

Response to Arguments

8. Applicant's arguments with respect to claims 1 and 13 have been considered but are moot in view of the new ground(s) of rejection.

After further consideration, it is determined that the new found reference of Potu in combination with Dea , and system of Dea, Abramatic et al., respectively , are applicable to the argued and claimed limitation as recited in claim 1 and 13 respectively. Thus a new ground of rejection is presented.

9. The papers filed on ***February 19, 2002*** (certificate of mailing dated ***February 4, 2002***) have not been made part of the permanent records of the United States Patent and Trademark Office (Office) for this application (37 CFR 1.52(a)) because of damage from the United States Postal Service irradiation process. The above-identified papers, however, were not so damaged as to preclude the USPTO from making a legible copy of such papers. Therefore, the Office has made a copy of these papers, substituted them for the originals in the file, and stamped that copy:

COPY OF PAPERS

ORIGINALLY FILED

If applicant wants to review the accuracy of the Office's copy of such papers, applicant may either inspect the application (37 CFR 1.14(d)) or may request a copy of the Office's records of such papers (*i.e.*, a copy of the copy made by the Office) from the Office of Public Records for the fee specified in 37 CFR 1.19(b)(4). Please do **not** call the Technology Center's Customer Service Center to inquiry about the completeness or accuracy of Office's copy of the above-identified papers, as the Technology Center's Customer Service Center will **not** be able to provide this service.

If applicant does not consider the Office's copy of such papers to be accurate, applicant must provide a copy of the above-identified papers (except for any U.S. or foreign patent

documents submitted with the above-identified papers) with a statement that such copy is a complete and accurate copy of the originally submitted documents. If applicant provides such a copy of the above-identified papers and statement within **THREE MONTHS** of the mail date of this Office action, the Office will add the original mailroom date and use the copy provided by applicant as the permanent Office record of the above-identified papers in place of the copy made by the Office. Otherwise, the Office's copy will be used as the permanent Office record of the above-identified papers (*i.e.*, the Office will use the copy of the above-identified papers made by the Office for examination and all other purposes). This three-month period is not extendable.

10. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Linus H. Lo whose telephone number is (703) 305-4039.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, John W. Miller, can be reached at (703) 305-4795.

Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

or faxed to:

(703) 872-9314 (for Technology Center 2600 only)

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Sixth Floor (Receptionist).

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the Technology Center 2600 Customer Service Office whose telephone number is (703) 306-0377.

lhl

May 1, 2002

JOHN MILLER
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